

Remarks

Claim rejections - 35 USC 102

Claims 1-20 are rejected under 35 USC 102(b) over Paniccia.

It is respectfully submitted that Paniccia does not disclose testing ESD performance. Paniccia specifically discusses the problems of debugging a new product (col. 1, lines 53-57). It then proposes a solution for determining voltage applied to a p-n junction by monitoring the electric field by monitoring the electro-absorption of a mode-locked laser (col. 7, lines 18-23). Nowhere does Paniccia describe or suggest ways of monitoring ESD performance of an IC device.

Claim 1, in contrast, specifically defines a method of monitoring ESD performance. This

is not a feature proposed in arguments or only in the specification, but is specifically mentioned in claim 1.

However, in order to further distinguish the present invention from Paniccia, claim 1 has been amended to include the step of comparing the amount of reflected light to the amount of reflected light from an I/O cell having good ESD performance (see page 4, lines 23-31). This step is clearly not present in Paniccia and is not suggested anywhere in Paniccia.

Since the remaining claims 2-20 depend from claim 1, they will include the new limitation, and are therefore also distinguishable over Paniccia.

As to claim 8, it is respectfully submitted that Paniccia does not mention averaging a number of measurements. Nevertheless, claim 8 has been amended to specify that the samples are taken at the same I/O signal voltage level. This further distinguishes from Paniccia which clearly discusses measurements at different electric fields and temperatures (Fig. 7 and col. 7, lines 7-17).

As to claim 15, it is respectfully submitted that Paniccia does not discuss any testing in pre-packaged form. The section referred to by the examiner (col. 5, lines 50-55) has to be read in the context of the rest of the sentence which clearly states that it is often necessary to do the testing while the chip is packaged. In other words the section specifically sets the context of the problem, namely testing a packaged device. This is used by Paniccia to justify the need of a laser. Nowhere does it mention or contemplate testing of unfinished devices.

As to claim 16, it is respectfully submitted that Paniccia does not disclose that the device includes only some of its layers. The section referred to by the examiner (col. 1, lines 62-67) merely states that a typical IC has multiple layers and that it is therefore difficult to access nodes buried deep in the chip. There is no mention of testing while there are only some of the layers formed.

Response to Arguments

Regarding argument a), it is respectfully submitted that the examiner's argument that ESD testing using a laser beam is known by those in the art is unsupported by any fact. The examiner is respectfully requested to provide support for his assertion, since there is no cited reference to

support this contention. In any event, claim 1 has been amended to clearly distinguish it over Paniccia and other IC testing references.

Regarding arguments b) and c): As has been discussed above, Paniccia does not disclose a device having only some of its layers (see arguments above).

Furthermore, it is respectfully submitted that Fig 7 and col. 8, lines 6-15 specify a mode-locked laser, not a continuous wave laser. In any event, all of the dependent claims depend from claim 1 and therefore include the limitations of claim 1, and are therefore, by that reason alone, distinguishable over the prior art.

In view of the amendment of claim 1 which specifically includes the limitation of comparing the light reflected to the light reflected from an I/O cell with good ESD performance, it is respectfully submitted that all of the claims are distinguishable over the prior art.

Allowance of the application is therefore respectfully requested.

Version with markings to show changes made

1. (Once amended) A method of testing the ESD performance of an IC device, comprising
probing the device with a laser beam, (and)
monitoring the amount of light reflected from the device, and
comparing the amount of light reflected to the amount of light reflected from an
I/O cell having good ESD performance.

8. (Once amended) A method of Claim 5, wherein several samples are taken of each probed
location, at the same I/O signal voltage level, and the results averaged.

Respectfully Submitted,

Dated: Feb. 18, 2003



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